```
/* This files provides address values that exist in the system */
/*
c:\altera\13.1\University_Program\Computer_Systems\DE1-SoC\DE1-SoC_Computer\app_soft
ware */

#define BOARD                                           "DE1-SoC"

/* Memory */
#define DDR_START                                       0x00000000
#define DDR_END                                 0x3FFFFFFF
#define A9_ONCHIP_START                 0xFFFF0000
#define A9_ONCHIP_END                   0xFFFFFFFF
#define SDRAM_START                             0xC0000000
#define SDRAM_END                                       0xC3FFFFFF
#define FPGA_ONCHIP_START               0xC8000000
#define FPGA_ONCHIP_END                 0xC8003FFF
#define FPGA_CHAR_START                 0xC9000000
#define FPGA_CHAR_END                   0xC9001FFF

/* Cyclone V FPGA devices */
#define LEDR_BASE                               0xFF200000
#define HEX3_HEX0_BASE                  0xFF200020
#define HEX5_HEX4_BASE                  0xFF200030
#define SW_BASE                                 0xFF200040
#define KEY_BASE                                        0xFF200050
#define PS2_BASE                                        0xFF200100
#define JTAG_UART_BASE                  0xFF201000
#define UART_BASE                               0xFF201000
#define TIMER_BASE                              0xFF202000
#define AUDIO_BASE                              0xFF203040

/* Cyclone V HPS devices */
#define HPS_GPIO1_BASE                  0xFF709000
#define HPS_TIMER0_BASE                 0xFFC08000
#define HPS_TIMER1_BASE                 0xFFC09000
#define HPS_TIMER2_BASE                 0xFFD00000
#define HPS_TIMER3_BASE                 0xFFD01000
#define FPGA_BRIDGE                             0xFFD0501C

/* ARM A9 MPCORE devices */
#define PERIPH_BASE                     0xFFFEC000              // base address of
peripheral devices

/* Interrupt controller (GIC) CPU interface(s) */
#define MPCORE_GIC_CPUIF                0xFFFEC100                              //
PERIPH_BASE + 0x100
#define ICCICR                                          0x00
                // offset to CPU interface control reg
```

```
#define ICCPMR                                          0x04
                // offset to interrupt priority mask reg
#define ICCIAR                                          0x0C
                // offset to interrupt acknowledge reg
#define ICCEOIR                                     0x10
        // offset to end of interrupt reg
/* Interrupt controller (GIC) distributor interface(s) */
#define MPCORE_GIC_DIST                 0xFFFED000                              //
PERIPH_BASE + 0x1000
#define ICDDCR                                          0x00
                // offset to distributor control reg
#define ICDISER                                     0x100
        // offset to interrupt set-enable regs
#define ICDICER                                     0x180
        // offset to interrupt clear-enable regs
#define ICDIPTR                                     0x800
        // offset to interrupt processor targets regs
#define ICDICFR                                     0xC00
        // offset to interrupt configuration regs

/* Private timer */
#define MPCORE_PRIV_TIMER               0xFFFEC600                              //
PERIPH_BASE + 0x0600
```

```
/* This files provides address values that exist in the system */
/*
c:\altera\13.1\University_Program\Computer_Systems\DE1-SoC\DE1-SoC_Computer\app_soft
ware */

/* Memory */
                        .equ    DDR_START,
0x00000000
                        .equ    DDR_END,
0x3FFFFFFF
                        .equ    A9_ONCHIP_START,                        0xFFFF0000
                        .equ    A9_ONCHIP_END,                          0xFFFFFFFF
                        .equ    SDRAM_START,                            0xC0000000
                        .equ    SDRAM_END,
0xC3FFFFFF
                        .equ    FPGA_ONCHIP_START,              0xC8000000
                        .equ    FPGA_ONCHIP_END,                        0xC8003FFF
                        .equ    FPGA_CHAR_START,                        0xC9000000
                        .equ    FPGA_CHAR_END,                          0xC9001FFF

/* Cyclone V FPGA devices */
                        .equ    LEDR_BASE,
0xFF200000
                        .equ    HEX3_HEX0_BASE,                         0xFF200020
                        .equ    HEX5_HEX4_BASE,                         0xFF200030
                        .equ    SW_BASE,
0xFF200040
                        .equ    KEY_BASE,
0xFF200050
                        .equ    JTAG_UART_BASE,                         0xFF201000
                        .equ    TIMER_BASE,                             0xFF202000

/* Cyclone V HPS devices */
                        .equ    HPS_GPIO1_BASE,                 0xFF709000
                        .equ    HPS_TIMER0_BASE,                        0xFFC08000
                        .equ    HPS_TIMER1_BASE,                        0xFFC09000
                        .equ    HPS_TIMER2_BASE,                        0xFFD00000
                        .equ    HPS_TIMER3_BASE,                        0xFFD01000
                        .equ    FPGA_BRIDGE,                            0xFFD0501C

/* ARM A9 MPCORE devices */
                        .equ    PERIPH_BASE,                            0xFFFEC000
        // base address of peripheral devices

                        /* Interrupt controller (GIC) CPU interface(s) */
                        .equ    MPCORE_GIC_CPUIF,       0xFFFEC100
// PERIPH_BASE + 0x100
                        .equ    ICCICR,                                         0x00
```

```
                                address_map_arm.s
                                // CPU interface control register
                        .equ    ICCPMR,                                         0x04
                                // interrupt priority mask register
                        .equ    ICCIAR,                                         0x0C
                                // interrupt acknowledge register
                        .equ    ICCEOIR,
0x10                                    // end of interrupt register
                        /* Interrupt controller (GIC) distributor interface(s) */
                        .equ    MPCORE_GIC_DIST,        0xFFFED000
// PERIPH_BASE + 0x1000
                        .equ    ICDDCR,                                         0x00
                                // distributor control register
                        .equ    ICDISER,
0x100                                   // interrupt set-enable registers
                        .equ    ICDICER,
0x180                                   // interrupt clear-enable registers
                        .equ    ICDIPTR,
0x800                                   // interrupt processor targets registers
                        .equ    ICDICFR,
0xC00                                   // interrupt configuration registers

                        /* Private timer interface(s) */
                        .equ    MPCORE_PRIV_TIMER,              0xFFFEC600
        // PERIPH_BASE + 0x0600
```

address_map_nios2.h

```
/*
c:\altera\13.1\University_Program\Computer_Systems\DE1-SoC\DE1-SoC_Computer\app_soft
ware */
#ifndef __ADDRESS_MAP__
#define __ADDRESS_MAP__

#define SDRAM_BASE 0x0
#define SDRAM_END 0x3fffffff
#define ONCHIP_SRAM_BASE 0x8000000
#define ONCHIP_SRAM_END 0x8003fff
#define EXPANSION_JP2_BASE 0xff200070
#define EXPANSION_JP1_BASE 0xff200060
#define PUSHBUTTON_BASE 0xff200050
#define SLIDER_SWITCH_BASE 0xff200040
#define HEX7_HEX4_BASE 0xff200030
#define HEX3_HEX0_BASE 0xff200020
#define RED_LED_BASE 0xff200000
#define PS2_PORT_BASE 0xff200100
#define PS2_PORT_DUAL_BASE 0xff200108
#define IRDA_BASE 0xff201020
#define JTAG_UART_BASE 0xff201000
#define INTERVAL_TIMER_BASE 0xff202000
#define SYSID_BASE 0xff202020
#define AV_CONFIG_BASE 0xff203000
#define VGA_PIXEL_BUFFER_CONTROL_REGISTER_BASE 0xff203020
#define VGA_CHAR_BUFFER_BASE 0x9000000
#define VGA_CHAR_BUFFER_END 0x9001fff
#define VGA_CHAR_BUFFER_CONTROL_REGISTER_BASE 0xff203030
#define AUDIO_SUBSYSTEM_AUDIO_BASE 0xff203040
#define
VIDEO_IN_SUBSYSTEM_EDGE_DETECTION_SUBSYSTEM_EDGE_DETECTION_ROUTER_CONTROLLER_BASE
0xff203070
#define VIDEO_IN_SUBSYSTEM_VIDEO_IN_DMA_BASE 0xff203060
#define VIDEO_IN_SUBSYSTEM_VIDEO_IN_DMA_END 0xff20306f
#define ADC_BASE 0xff204000

#endif
```

```
/*
c:\altera\13.1\University_Program\Computer_Systems\DE1-SoC\DE1-SoC_Computer\app_soft
ware */
.equ SDRAM_BASE, 0x0
.equ SDRAM_END, 0x3fffffff
.equ ONCHIP_SRAM_BASE, 0x8000000
.equ ONCHIP_SRAM_END, 0x8003fff
.equ EXPANSION_JP2_BASE, 0xff200070
.equ EXPANSION_JP1_BASE, 0xff200060
.equ PUSHBUTTON_BASE, 0xff200050
.equ SLIDER_SWITCH_BASE, 0xff200040
.equ HEX7_HEX4_BASE, 0xff200030
.equ HEX3_HEX0_BASE, 0xff200020
.equ RED_LED_BASE, 0xff200000
.equ PS2_PORT_BASE, 0xff200100
.equ PS2_PORT_DUAL_BASE, 0xff200108
.equ IRDA_BASE, 0xff201020
.equ JTAG_UART_BASE, 0xff201000
.equ INTERVAL_TIMER_BASE, 0xff202000
.equ SYSID_BASE, 0xff202020
.equ AV_CONFIG_BASE, 0xff203000
.equ VGA_PIXEL_BUFFER_CONTROL_REGISTER_BASE, 0xff203020
.equ VGA_CHAR_BUFFER_BASE, 0x9000000
.equ VGA_CHAR_BUFFER_END, 0x9001fff
.equ VGA_CHAR_BUFFER_CONTROL_REGISTER_BASE, 0xff203030
.equ AUDIO_SUBSYSTEM_AUDIO_BASE, 0xff203040
.equ
VIDEO_IN_SUBSYSTEM_EDGE_DETECTION_SUBSYSTEM_EDGE_DETECTION_ROUTER_CONTROLLER_BASE,
0xff203070
.equ VIDEO_IN_SUBSYSTEM_VIDEO_IN_DMA_BASE, 0xff203060
.equ VIDEO_IN_SUBSYSTEM_VIDEO_IN_DMA_END, 0xff20306f
.equ ADC_BASE, 0xff204000
```